1.8V, 32/64/128/256byte EEPROM IP Macro Block
For 0.18um CMOS Process of Key-Foundry
Product Code: WC18EP1-32/64/128/256

1. General Description

Key features

- 1.8V Single power supply : 1.62V ~ 1.98V
- Read Frequency : 1MHz
- x8 read output
- Low active current : 1mA (max.) at 1MHz
- Low write current: 2mA (max.)
- Erase : 4msec (typical)
- Program : 4msec (typical)
- Main functions : read, erase, and program
- Test modes: even/odd /all byte-erase, even/odd/all byte-program.
- Device reset by RSTn pin (during power-up)
- Data retention : More than 10 years
- E/W cycle endurance: Min. 1K

“WC18EP1” is a 2P4M (two-poly, four-metal) and MIM(M2-M3), non-volatile EEPROM Macro IP block which is embedded into the 0.18um standard CMOS process of Key-Foundry.

Fig 1. Circuit block diagram

Circuit Block Diagram

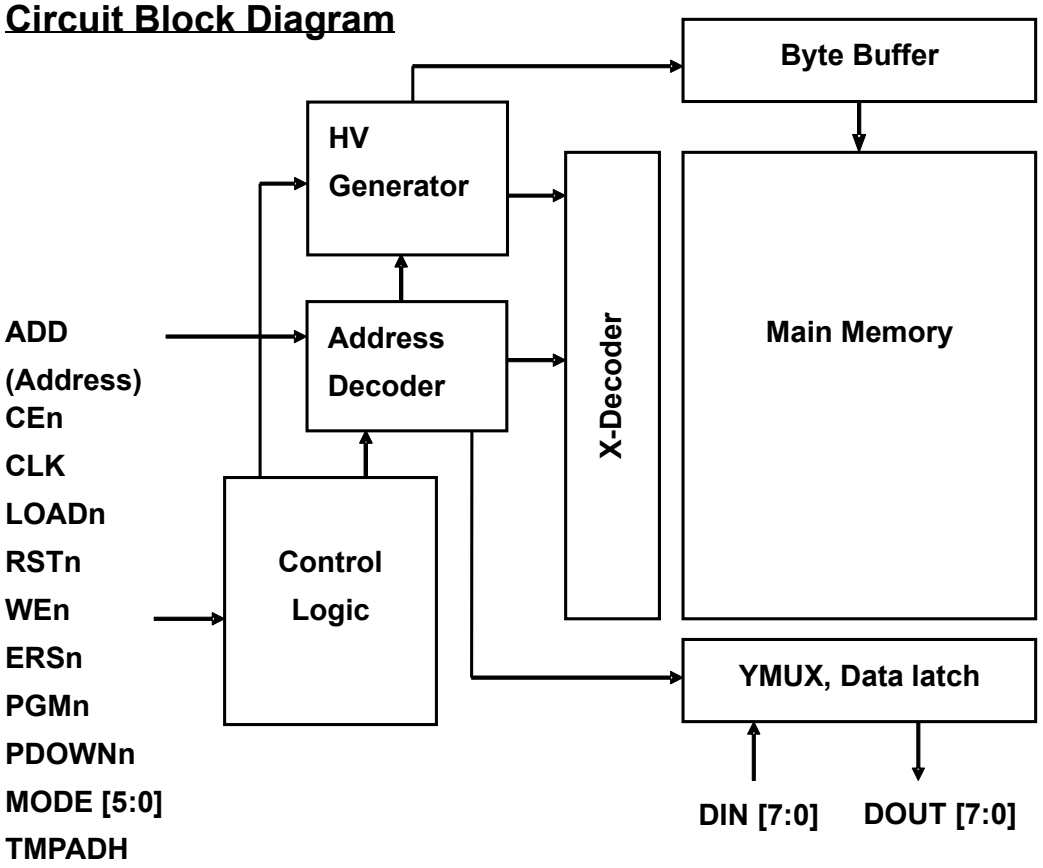


Table 1. Signal description

Symbol	Pin name	Function
MODE[5:0]	Mode select bits	To select the functional modes
ADD[7:0]	Address inputs	Memory addresses.
DIN [7:0]	Data inputs	To receive input data for write.
DOUT[7:0]	Data outputs	Output data from EEPROM IP.
CEn	Chip Enable	To activate the EEPROM macro device.
CLK	Clock	To Read the Main Array.
WEn	Write Enable	To control write operations.
RSTn	Reset Enable	To reset the device during power-up or terminate any operation under progress. All internal registers including the byte buffer are reset by RSTn.
LOADn	Load Enable	To load data into byte buffer for a write operation
ERSn	Erase Enable	To erase the main array.
PGMn	Program Enable	To program the main array.
PDOWNn	Power Down Enable	“PDOWNn=Low” forces the IP block to enter “power down mode”. In this mode, the current consumption is deeply suppressed down to 1uA, typically
TMPADH	Test Pin	Test PAD

Note 1) A_{MS} : The Most Significant Address Bit

2. Functional Modes

Two groups of functional modes are provided: **Main modes** and **Test Modes**. These functions can be selected by MODE [5:0] as shown in the table 2. Main functions are composed of five functions: Reset, Stand-by, Read, Erase and Program. These main functions are enough to meet almost all functional requirements of the normal customers for their various applications. On the other hand, test modes can be usefully utilized in many cases like customer’s production test.

Table 2. Functional modes and Mode selection bits (MODE[5:0])

Mode	Functions		MODE [5:0]
Main Mode	Reset		don't care
	Standby		
	Read		0h
	Byte-erase (load + erase)		0h
	Byte-program (load + program)		0h
Test Mode	Erase	Even Byte-erase	1h
		Odd Byte-erase	2h
		All Byte-erase (Bulk erase)	3h
	Program	Even Byte-program	1h
		Odd Byte-program	2h
		All Byte-program (Bulk program)	3h
	Measure	VREAD Measure	4h
		VPP Measure	8h
		Cell Current Measure	34h
	Verify	Program verify	0h
		Erase verify	0h

Table 3. Pin description and status for main modes

	Main Modes						
	Power Down	Reset	Standby	Read	Write operations		
					Load	Byte-erase	Byte-program
MODE[5:0]	x	x	x	0h	**0h**	**0h**	**0h**
ADD [byte]	x	x	x	Ain	Ain	Ain	Ain
Din[7:0]	x	x	x	x	Din	x	x
DOUT[7:0]	x	x	x	Dout	x	x	x
CEn	x	x	H	L	L	L	L
CLK	x	x	x	Toggle	x	x	x
WEn	x	x	x	H	Toggle	L	L
ERSn	x	x	x	H	H	L	H
PGMn	X	X	X	H	H	H	L
LOADn	x	x	x	H	L	H	H
RSTn	H	L	H	H	H	H	H
PDOWNn	L	H	H	H	H	H	H

(Note 1) x (Don't care): Vil or Vih for input, Vol or Voh for output
(Note 2) Ain : Address Input
(Note 3) ATD (Address Transition Detect) signal is generated by CLK pulse (Toggle) in read operation

3. Read

The EEPROM Macro device automatically enters the read mode after power-up. During power-up, RSTn (Device Reset Signal) should be kept low to correctly initialize the device.

The device has three control pins (CEn and CLK) for read, which must be correctly asserted in order to obtain valid data at the outputs. Chip Enable (CEn) is used for enable the device. CLK is used to generate an internal ATD (Address Transition Detect) for the input addresses.
In case that addresses are kept stable, tAA is defined as a delay from the falling edge of CLK to the valid data output.
Resultantly, actual read access time is defined as "tCLKH+tAA".

Fig 2. Read Operation Timing Diagram

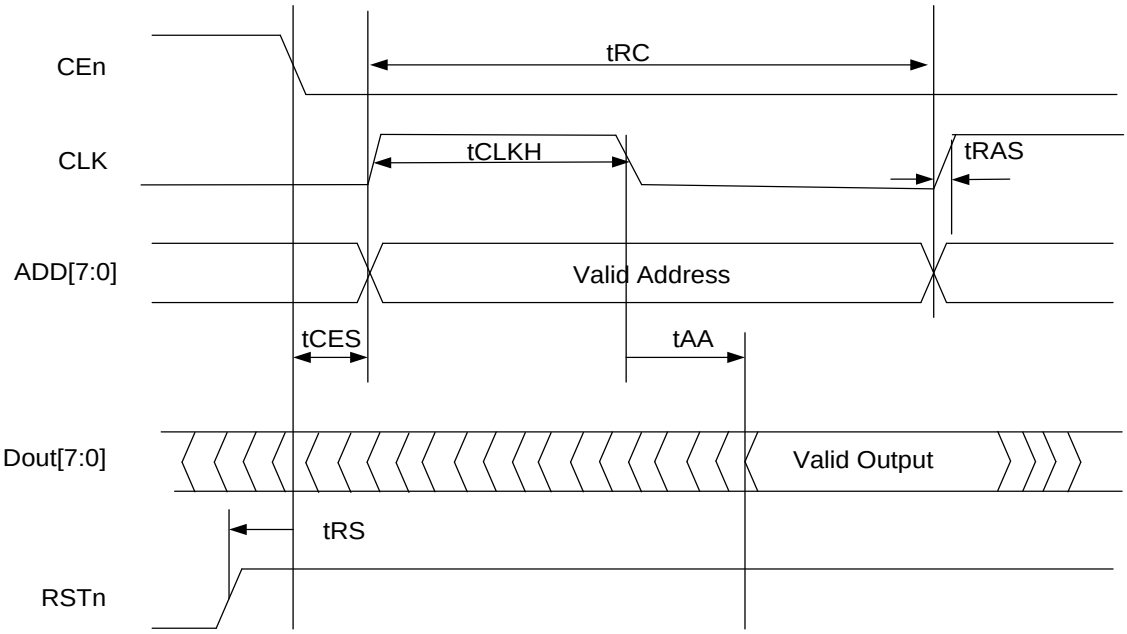


Table 4.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRC	Read Cycle Time	1000			ns
	Read Cycle Frequency			1	MHz
tCLKH	CLK High Time	400			ns
tRAS	Read Address Setup Time	0			ns
tAA	Address Access Time			50	ns
tCES	CEn Setup Time	1000			ns
tRS	RSTn Setup Time	100			ns

Note 1) For read access time, **Cload** (Load Capacitance at output) is assumed to be less than **0.3pF**.

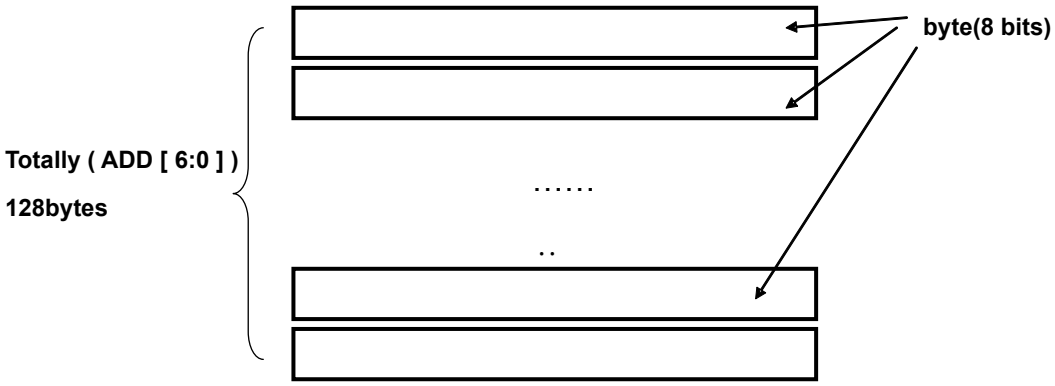
4. Physical organization of Main memory

A byte is composed of 8 bits. The whole memory array is composed of 32 bytes. Refer to table 5 and Fig. 3 to see how physically the whole memory array is organized.

Table 5. Memory organization table

Product code	Memory size (Bytes)	Byte size	Byte address
WC18EP1_32	32	8 bits	ADD[4:0]
WC18EP1_64	64	8 bits	ADD[5:0]
WC18EP1_128	128	8 bits	ADD[6:0]
WC18EP1_256	256	8 bits	ADD[7:0]

Fig. 3 Organization of the whole memory array



5. Write Operation

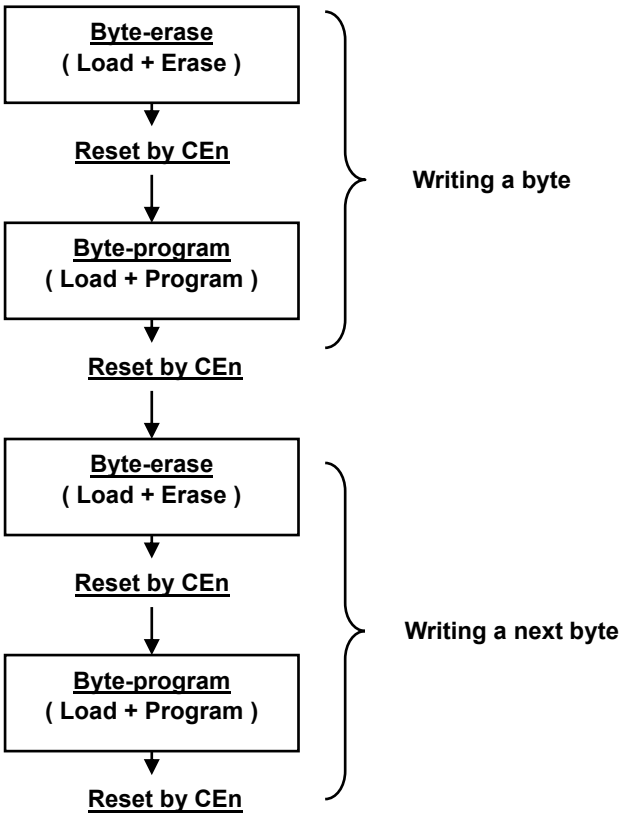
In this macro block, two types of write operation are provided: **Byte-erase** and **Byte-program**. Each write operation is composed of two cycles. Here, “write operation” means either “erase” or “program”, or both.

- Byte-erase = Load + Erase (by ERSn and WEn)
- Byte-program = Load + Program (by PGMn and WEn)

To correctly write data into the main memory, a byte data should be first loaded with a specific address into an internal 8-bit register called a **byte-buffer**. This “data load operation” is performed during **“Load cycle”**. And then **“**erase” or “program**”** can be selectively executed by users. Erase operation is controlled by **ERSn with WEn** and program operation is controlled by **PGMn with WEn**.
This macro block requires typically 4msec for erase or program respectively. But, the write time can be freely controlled by keeping ERSn or PGMn and WEn signals at low as long as users want. Refer to Fig.5 for write operation timing.

A normal write operation sequence is depicted in Fig.4. As shown clearly in the diagram, “Device reset (by CEn)” is strongly recommended between the first write and the second write. The byte-buffer (a kind of internal register into which data is loaded) needs to be completely cleared before moving to next write. Otherwise, the next byte date can be written over the previous data which was loaded during the previous write operation. This “over-written data” can generate “unwanted results”. The byte-buffer is cleared when CEn is driven from low to high.

Fig. 4 Normal Write Operation Sequence



Write Operation

Typically 4msec (tWRITE) is enough for erase or program respectively.
It should be noted that the byte address is kept stable for the whole write operation, as shown in the Fig.5. Actual write time (tWRITE) can be freely adjusted by users by keeping ERSn or PGMn and WEn at low as long as users want.

Recovery Time (tRHCH) from Write

After a write operation is completed, the device automatically returns to “normal read mode”. But, 20usec of recovery time (tRHCH) is needed for the device gets ready for read or other operation.

Terminated Write by “CEn Reset”

When the device is forced to be reset by CEn while a write operation is still going on, the write operation is immediately terminated and returns to “normal read mode”. But, in this case, 20usec of recovery time is needed for the device to get ready for read.

Fig. 5 Write Operation

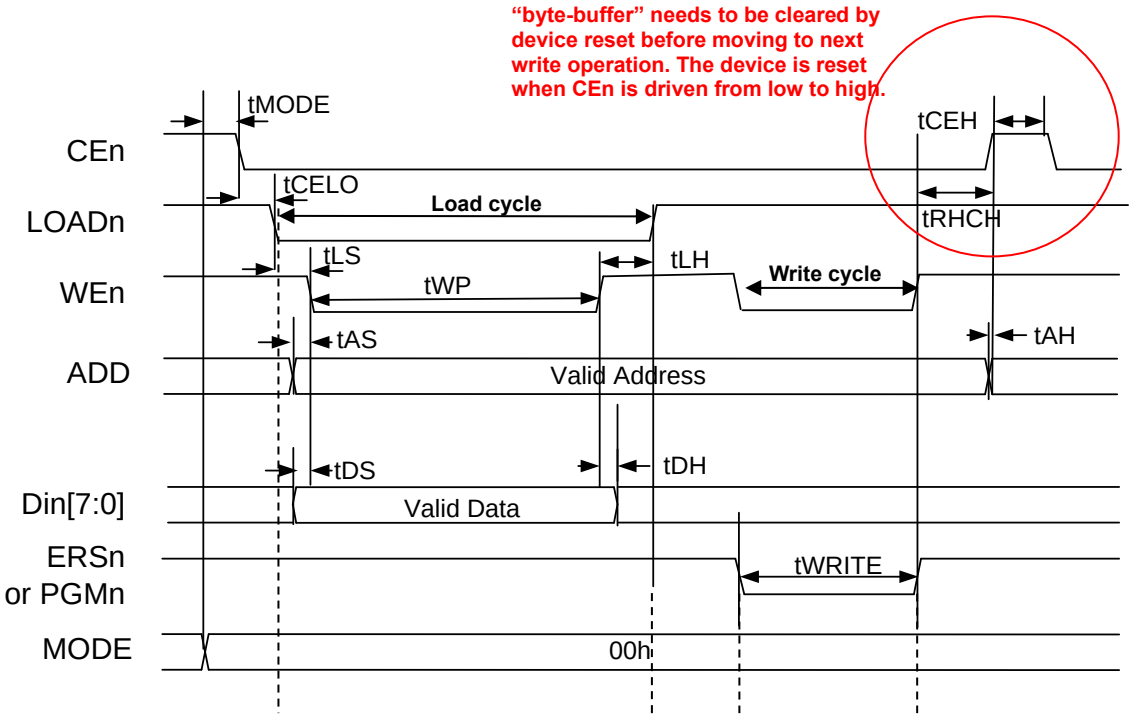


Table. 6

Symbol	Parameter		Min.	Typ.	Max.	Unit
tWP	WEn Low Width		50			ns
tAS	Address Setup Time		100			ns
tAH	Address Hold Time		100			ns
tDS	Data Input Setup time		100			ns
tDH	Data Input Hold time		100			ns
tMODE	MODE pin Setup Time		0			ns
tCELO	CEn Low to LOADn Low time		0			ns
tCEH	CEn High Width		100			ns
tLS	LOADn Setup Time		100			ns
tLH	LOADn Hold Time		100			ns
tRHCH	Write end to CEn High Time		20			us
tWRITE	Write Time	Byte-erase	3	4	8	ms
		Byte-program	3	4	8	ms

Loading Data and Address by WEn

During data load operation, data is latched at the rising edge of WEn. But, data should be kept stable during the low period of WEn. Otherwise, wrong data can be latched.
On the other hand, address is not latched so that it should be kept stable for the whole period of write operation.

Dummy data for Erase

Any data (one byte) should be loaded into the byte-buffer for erase. If nothing is loaded during the load cycle, nothing is erased. The value or pattern of data does not have any meaning. Just a dummy data (including “00h”) is acceptable.

Data ‘Over-write”

Sometimes, new data can be over-written onto the previous data in the main memory array during the byte-program operation. This is the so-called “over-write” or “over-programming”. Only “0” can be changed to “1” while “1 bit” can not return to “0” by byte-program operation. Instead, “1’ can return to “0” only by performing “erase operation”.
Therefore, a byte location needs to be “erased” first by “erase operation” before any byte-program is performed on the same location, in order to keep integrity of data.

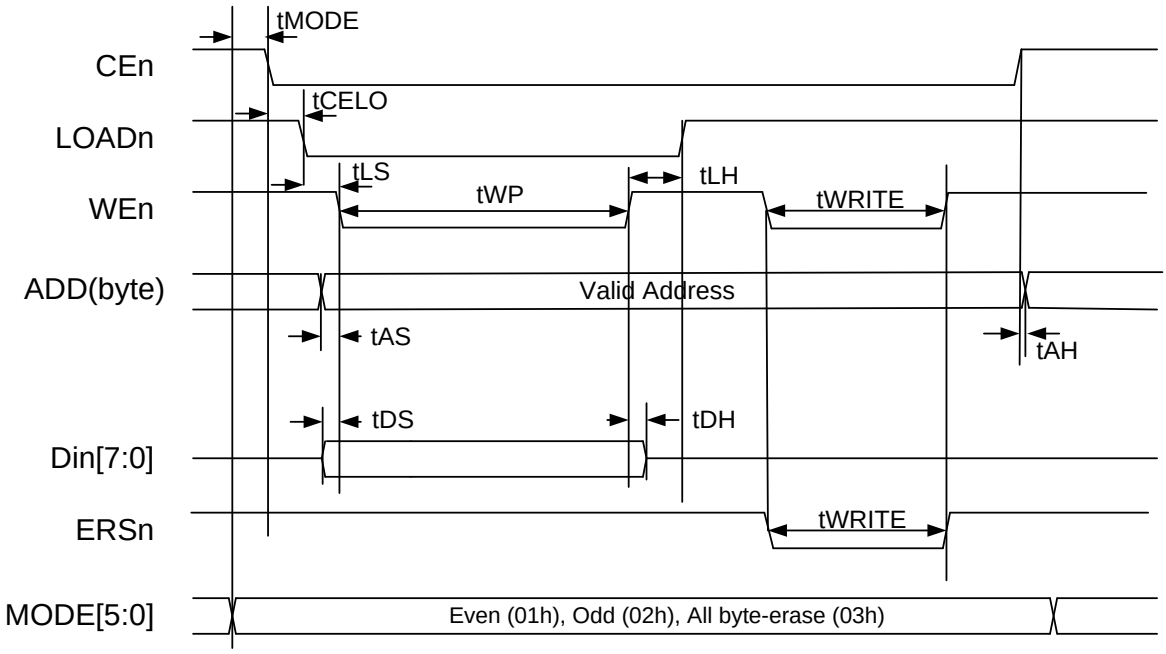
6. Test Modes (Erase)

Three test erase-modes (even, odd and all byte-erase) are additionally provided for more flexible user application and test-time reduction, and they can be selected by MODE [5:0] as shown in the table 7 below. Each test erase mode is functionally the same as **byte-erase** operation of the main mode, except that the scopes of bytes supported by test modes are different from the main mode, as shown in the table 7 below.

Table 7.

Type	Modes	MODE [5:0]	Scope of bytes to erase
Main mode	Byte-erase	0h	Any single byte designated by a byte-address
Test mode	Even byte-erase	1h	All bytes only with even byte-address (byte #0, #2, #4…)
	Odd byte-erase	2h	All bytes only with odd byte-address (byte #1, #3, #5...)
	All byte-erase (**Bulk erase**)	3h	All bytes (Whole memory block)

Fig. 8 Timing diagram for the test erase-modes



7. Test Modes (Program)

Three test program-modes (even, odd, and all byte-program) are additionally provided for more flexible user application and test-time reduction, and they can be selected by MODE[5:0] as shown in the table 7 below. Each test program mode is functionally the same as the byte-program operation of the main mode, except that the scopes of bytes supported by the test modes are different from the main mode, as shown in the table 8 below.

In the even byte-program mode, the same data loaded in the byte-buffer is repeatedly copied (programmed) into all bytes with even address in the whole memory block.
In the odd byte-program mode, the same data loaded in the byte-buffer is repeatedly copied (programmed) into all bytes with odd address in the whole memory block.
On the other hand, the whole memory block can be programmed at once with the same data pattern by performing “all byte-program (bulk program)”.

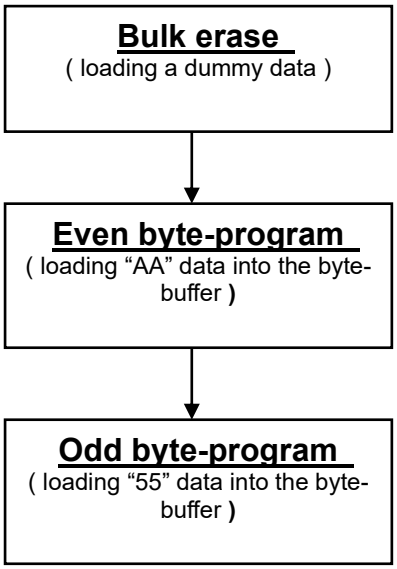
Table 8.

Type	Modes	MODE [5:0]	Scope of bytes to program
Main mode	Byte-program	0h	Any single byte designated by a byte-address
Test mode	Even byte-program	1h	All bytes only with even byte-address (byte #0, #2, #4…)
	Odd byte-program	2h	All bytes only with odd byte-address (byte #1, #3, #5...)
	All byte-program (**Bulk program**)	3h	All bytes (Whole memory block)

How to generate “CKB (Checker Board) pattern” by using the test modes

A CKB pattern can be easily and fast generated by properly using the test mode functions.
Refer to the block diagram (Fig. 9) below.
First, “bulk erase” is performed. And then, an even byte-program is executed with data “AA”. And then, an odd byte-program is executed with data “55”. Then, “full CKB pattern” will be easily obtained over the whole memory block. The total write time for the full CKB pattern is about 7.5msec (typically): bulk erase (4msec), even byte-program (4msec), and odd byte-program (4msec).

Fig. 9 Fast Generation Flow for a Full CKB pattern



8. Verify Mode

In the test mode, two special read modes are provided: **erase-verify** and **program-verify**. But, from the functional point of view, there is almost no difference between verify (test mode) and read (main mode). These are provided for testing or debugging purpose.
When PGMn is low, “program-verify” is activated, while “erase-verify” is activated by “ERSn”.

Fig. 9 Verify timing diagram

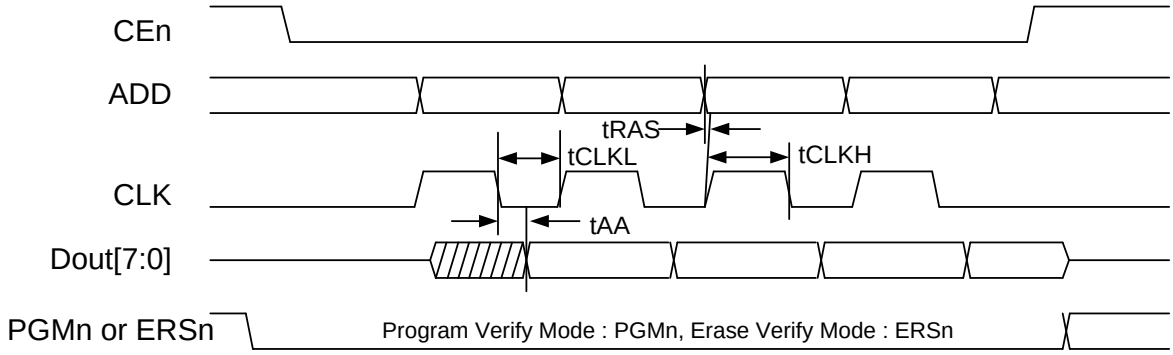


Table 10.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLKL	CLK Pulse Low Width	400			ns
tRAS	Address Set-up Time	0			ns
tAA	CLK to Valid Output Time			50	ns
tMODE	MODE pin Setup Time	0			ns
tCLKH	CLK Pulse High Width	400			ns

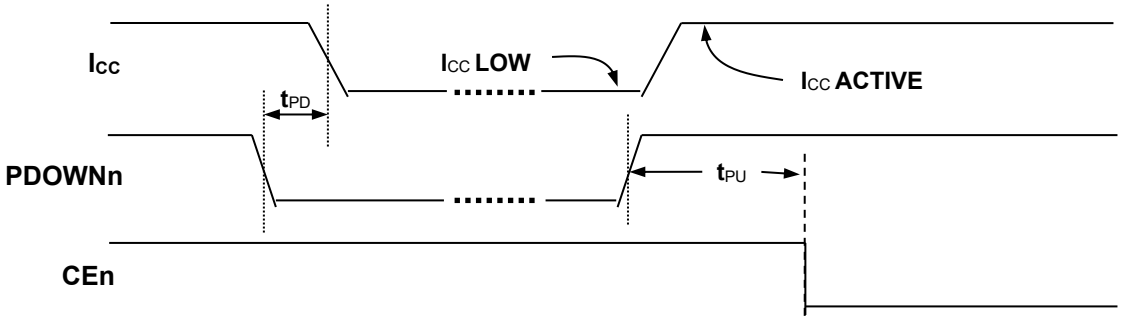
9. Stand-by Mode

When CEn is driven to high, the device goes to “stand-by mode”, in which all internal circuits of the device is completely disabled and all outputs become X (Unknown Data). In this stand-by state, only intrinsic leakage current caused by process itself flows through the entire device.

10. Deep power-down mode

In case that extremely small power consumption is required in stand-by mode, the deep power-down mode is recommended. In this mode, typically less than 1uA is consumed. By just asserting low to PDOWNn input, the device can be forced to enter the deep mode. In this mode, all circuits are completely turned off. At the same time, all internal registers and latches including the page buffer are reset to all "0". Furthermore, any in-progress operation (such as write operation) is immediately terminated. However, 100usec of wake-up time is required for the device to return to the normal read mode after the device gets out of this deep power-down mode.

Fig. 10 Deep power-down mode



11. Device Reset

The device can be reset by asserting RSTn **(at least 100nsec, tRSTL**), regardless of other control signals (CEn, WEn). All internal registers and latches including the **byte buffer** are completely cleared (initialized) and all outputs turn to X (Unknown) by the device reset. While the device stays at reset status (RSTn at low), all internal circuits of the device are disabled. So, in this reset status, just intrinsic leakage current (called "stand-by current") is consumed over the entire device, like the stand-by mode.
In order to guarantee the safe device operation during power-up, the device needs to stay at reset status by keeping RSTn low until the power-supply is fully ramped up and finally stabilized. Refer to Fig.11. If the device is not kept properly at reset during power-up, some undesired result may take place by unstable input signals or noises generated during power-up.
After power-up, the device automatically enters the read mode. But, **100usec** of wait-time (tSR) is required for the device to get ready for read even if the device gets out of "device reset" by releasing RSTn.
In case that RSTn is asserted during the write operation, the write operation will be immediately interrupted and terminated. Therefore, they (the interrupted operations) need to be reinitiated to ensure data integrity which may have been corrupted by immediate termination of the write process.

Fig. 11 Device reset during power-up and power-down

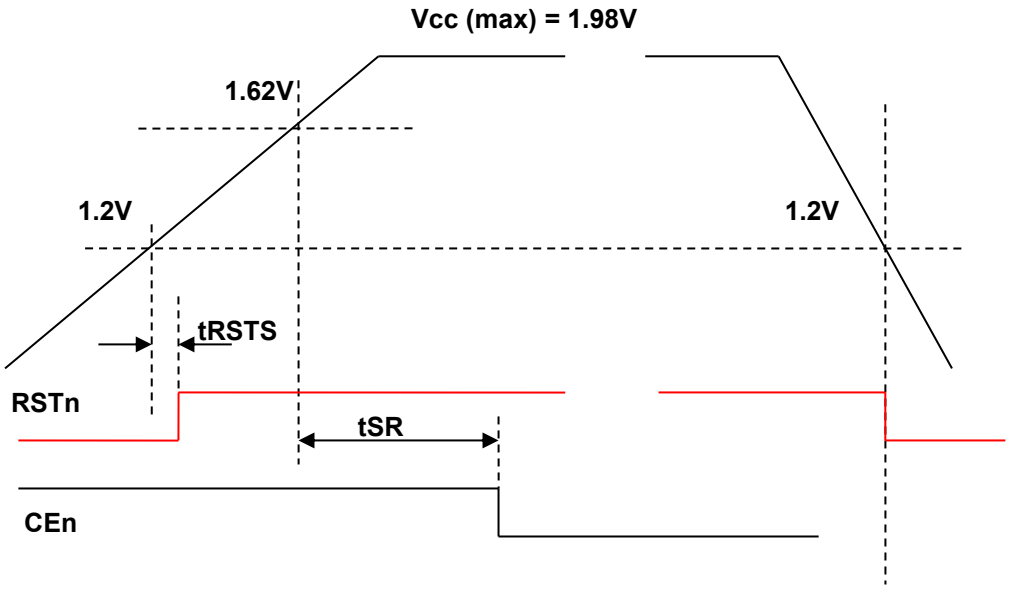


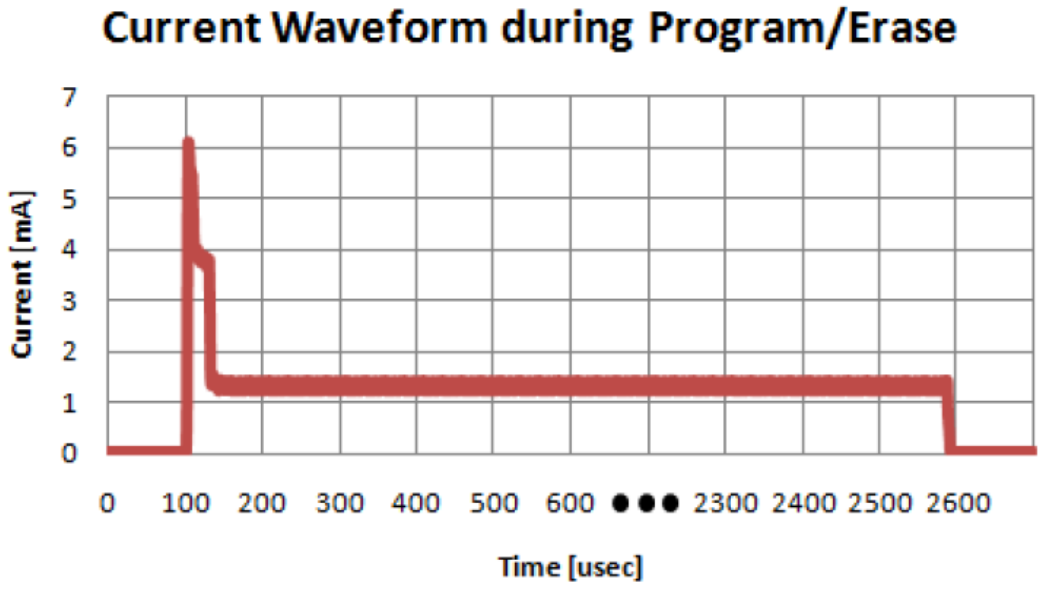
Table 13.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tPD	Power Down Time			5	us
tPU	Power Up Time	100			us
tRSTS	RSTn Set Time	0			ns
tRSTL	RSTn Low Width Time	100			ns
tSR	System Ready during power up	100			us

12. Peak current during write operation

For the write operation, an internal charge-pump circuit is activated and a peak current occurs for a short period of time just at the initial phase of the write operation. Refer to Fig.11.
As shown in Fig 12, **6mA** of peak current at maximum can flow from VDD. This initial peak current is caused by activating charge pump circuit to generate high voltages for cell array into which data will be written. However, the peak-current is rapidly suppressed down to less than 1.5mA as soon as the internal charge pump operation is stabilized.
Even if the supplying current to the device is limited to 4mA, actual write operation is not critically affected.

Fig. 12 A peak current during write operation (through VDD power supply)



13. DC Operating Characteristics

Table 14.

Description	Symbol	Condition	Min	Typ	Max	Unit
Operation Temperature	Temp.	Read	-40	25	85	℃
		Write	-20	25	85	
Power Supply Voltage	V_{DD}	Read	1.62	1.8	1.98	V
Stand By Current	I_{SB}	CEn= High		20	100	μA
Power Down Current	Ipd	PDOWNn=Low		1	50	μA
Read Current (Output Disabled)	I_{CC}	1MHz			1	mA
Write Current	I_{WR}	Erase or Program		2	5	mA
Input Low Voltage	V_{IL}		-0.5	0	0.5	V
Input High Voltage	V_{IH}		V_{DD} -0.5	V_{DD}	V_{DD} +0.5	V
Output High Voltage	V_{OH}	Ioh=1uA	$0.9XV_{DD}$		$1.1XV_{DD}$	V
Output Low Voltage	V_{OL}	Iol=1uA	$-0.1XV_{DD}$		$0.1XV_{DD}$	V
Input Capacitance	C_{IN}	V_{IL}=0V; Temp. 25℃			0.1	pF
Output Capacitance	C_{OUT}	V_{IL}=0V; Temp. 25℃			0.3	pF

Revisions

Revision No: Rev.A (Draft)
Dec 2, 2015
Revised by S.D Kim (sdkim@Jeenix.com)
Initial release of the datasheet (preliminary version)

Revision No: Rev.B0
Dec. 29, 2020
Revised by S.D Kim (sdkim@Jeenix.com)

1. Deep Power Down Mode Added (Fig.10) → Page 13.
2. Magnachip → Key-Foundry
3. Compony Address Changed

Note

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